second 20/22 regions. An exemplary N-Well implant is 2.8 to 3.0 x 10^{12} impurities/cm^2 of phosphorous at 160 keV of energy. Then in step 62 and Fig. 5C, a first protective coating 132 is applied over the first and second 20/22 regions. An exemplary first protective coating is field oxide (FOX). Then in step 64 and Fig. 5C, the first conductivity dopant [126]128 is driven into the substrate to form regions 132 by baking the substrate 10, such as at 1200°C for 4 hours. Then in step 66, the first dielectric layer 124 is removed. Then in step 68 and Fig. 5D, a defined deposition of a second dielectric layer 136 is created in the same location as the defined deposition of the first dielectric layer 124, such as channel oxide. Then in step 70 and Fig. 5D, a second conductivity dopant 138 is implanted in the substrate 10 as second conductivity implant 134 and disposed under the defined deposition of the second dielectric layer 136. An exemplary second conductivity dopant 138 is boron at a concentration of 9.8 x 10^{12} impurities/cm^2 at an energy of 33 keV. Then in step 72 and Fig. 5E, the second conductivity implant 134 is driven into the substrate10 to form a driven second conductivity implant 140, preferably by baking the substrate 10 at 1200°C at 4 hours. Then in step 74 and Fig. 5E, the first protective coating 132 and the second dielectric layer 136 are removed, for example, by using an oxide strip. Then in step 76 and Fig. 5F, a patterned third dielectric layer 146 is created over the surface of the substrate to expose the drain and source of the first 28 and second 26 conductivity low-voltage transistors and the first conductivity high-voltage transistor 30. The third dielectric layer 146 can be made of one or more dielectric layers. An exemplary third dielectric layer is made up of 200 Angstroms of SRO and 900 Angstroms of silicon nitride. Then in step 78, a defined deposition of a fourth dielectric layer 148 is created and disposed on the drain and source of the first conductivity low-voltage transistor 28. Then in step 80 and Fig. 5G, a second protective coating 150, for example photoresist, is applied over the first 142 and second 144 wells. Then in step 82 and Fig. 5H, a second conductivity field dopant 152 is implanted into the substrate and disposed under the drain and source of the first conductivity low-voltage transistor 28. An exemplary concentration of the second conductivity field dopant 152 is boron at a concentration of 8.5 x 10^{12} impurities/cm^2 at and energy of 120 keV. Then in step 84, the second protective coating 150 is removed. Then in